WHAT IS CLAIMED IS:

- 1. A magnetic random access memory (MRAM) device, comprising: a magnetic tunnel junction (MTJ) stack located over a substrate; a conductive layer located proximate the MTJ stack and over the substrate; and a low-k dielectric layer interposing the conductive layer and the MTJ stack.
- 2. The MRAM device of claim 1 wherein the conductive layer interposes the substrate and the MTJ stack.
- 3. The MRAM device of claim 1 wherein the MTJ stack interposes the substrate and the conductive layer.
 - 4. The MRAM device of claim 1 wherein the conductive layer is a program line.
 - 5. The MRAM device of claim 1 wherein the conductive layer is a bit line.
- 6. The MRAM device of claim 1 wherein the low-k dielectric layer comprises Black Diamond.
- 7. The MRAM device of claim 1 wherein the low-k dielectric layer has a thickness ranging between about 200 angstroms and about 2000 angstroms.
- 8. The MRAM device of claim 1 wherein the low-k dielectric layer comprises a material having a dielectric constant of about 3.9 or less.
- 9. The MRAM device of claim 1 wherein the low-k dielectric layer comprises a material having a dielectric constant of about 2.8 or less.

- 10. The MRAM device of claim 1 wherein the low-k dielectric layer comprises a material having a dielectric constant of about 2.0 or less.
 - 11. A magnetic random access memory (MRAM) device, comprising:
 - a magnetic tunnel junction (MTJ) stack located over a substrate;
 - a first conductive layer contacting the MTJ stack;
 - a second conductive layer proximate the first conductive layer; and
 - a low-k dielectric layer interposing the first and second conductive layers.
- 12. The MRAM device of claim 11 wherein the first conductive layer interposes the substrate and the second conductive layer.
- 13. The MRAM device of claim 11 wherein the second conductive layer interposes the substrate and the first conductive layer.
- 14. The MRAM device of claim 11 further comprising a substrate, wherein the MTJ stack interposes the substrate and, collectively, the first and second conductive layers and the low-k dielectric layer.
- 15. The MRAM device of claim 11 wherein one of the first and second conductive layers is a program line.
- 16. The MRAM device of claim 11 wherein one of the first and second conductive layers is a bit line.
- 17. The MRAM device of claim 11 wherein the low-k dielectric layer comprises Black Diamond.

- 18. The MRAM device of claim 11 wherein the low-k dielectric layer has a thickness ranging between about 200 angstroms and about 2000 angstroms.
- 19. The MRAM device of claim 11 wherein the low-k dielectric layer comprises a material having a dielectric constant of about 3.9 or less.
- 20. The MRAM device of claim 11 wherein the low-k dielectric layer comprises a material having a dielectric constant of about 2.8 or less.
- 21. The MRAM device of claim 11 wherein the low-k dielectric layer comprises a material having a dielectric constant of about 2.0 or less.
 - 22. A magnetic random access memory (MRAM) device, comprising:a first magnetic tunneling junction (MTJ) stack located over a substrate;a second MTJ stack located over the substrate and laterally opposing the first MTJ stack;
 - a low-k dielectric material electrically isolating the first and second MTJ stacks.

and

- 23. The MRAM device of claim 22 wherein the first and second MTJ stacks are substantially coplanar.
- 24. The MRAM device of claim 22 wherein the low-k dielectric layer comprises Black Diamond.
- 25. The MRAM device of claim 22 wherein the low-k dielectric layer comprises a material having a dielectric constant of about 3.9 or less.

- 26. The MRAM device of claim 22 wherein the low-k dielectric layer comprises a material having a dielectric constant of about 2.8 or less.
- 27. The MRAM device of claim 22 wherein the low-k dielectric layer comprises a material having a dielectric constant of about 2.0 or less.
 - 28. An integrated circuit device, comprising:
 - a substrate having a transistor located at least partially therein;
 - a first conductive layer located over the substrate;
 - a first dielectric layer interposing the first conductive layer and the substrate;
 - a magnetic tunneling junction (MTJ) stack located over the first conductive layer;
 - a second dielectric layer interposing the MTJ stack and the first conductive layer;
 - a third conductive layer located over the MTJ stack; and
 - a third dielectric layer interposing the third conductive layer and the MTJ stack;
- wherein at least a portion of at least one of the second and third dielectric layers proximate the MTJ stack comprises a low-k dielectric material.
- 29. The integrated circuit device of claim 28 wherein the low-k dielectric layer comprises Black Diamond.
- 30. The integrated circuit device of claim 28 wherein the low-k dielectric layer comprises a material having a dielectric constant of about 3.9 or less.
- 31. The integrated circuit device of claim 28 wherein the low-k dielectric layer comprises a material having a dielectric constant of about 2.8 or less.
- 32. The integrated circuit device of claim 28 wherein the low-k dielectric layer comprises a material having a dielectric constant of about 2.0 or less.